In re Patent Application of
POIROUX ET AL.
Serial No. **NOT YET ASSIGNED**
Filed: **HEREWITH**
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In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-24 (canceled).

25. (new) A method for evaluating a CMOS logic cell manufactured in partially depleted silicon-on-insulation (PD-SOI) technology, the logic cell including transistors having a floating substrate, the method comprising:

modeling the logic cell; and

determining internal potentials of the logic cell by

utilizing a stimulation signal in an operational simulation of the modeled logic cell, and

injecting the floating substrate of each transistor, at predetermined successive instants of injection, with a charge proportional to a variation of an internal potential of the corresponding transistor determined during a predetermined time interval of the stimulation signal preceding a current instant of injection.

26. (new) A method as claimed in Claim 25, wherein an injection current corresponding to the injected charge is determined such that, after injection, the variation of the internal potential of the corresponding transistor reaches n times a measured variation of the internal potential.

27. (new) A method as claimed in Claim 26, wherein the value of n is determined by measuring the variation of the internal potential of a transistor of the cell, during a cycle of the stimulation signal, and from an estimated amplitude of the variation of the internal potential of this transistor between a static equilibrium state and a dynamic equilibrium state.

28. (new) A method as claimed Claim 25, wherein the charge proportional to the variation of the internal potential of the corresponding transistor is determined using a proportionality coefficient having a value determined by measuring the variation of the internal potential and by the charge variation of a transistor of the logic cell during a cycle of the stimulation signal, and of a duration of injection.

29. (new) A method as claimed in Claim 25, wherein the stimulation signal comprises, in each period, a transition separating two plateaus, with an injection instant being located during a plateau and at a transition distance, and wherein the duration of injection of the current is selected to be greater than a time of the operational simulation and less than a duration of the plateau.

30. (new) A method as claimed in Claim 25, wherein consecutive injection instants are spaced at an interval equal to two periods of the stimulation signal, and wherein the time interval has a duration equal to a period of the stimulation

signal.

31. (new) A method as claimed in Claim 30, wherein an initial instant of the time interval precedes the injection instant of 1.5 periods of the stimulation signal, and a final instant of the time interval precedes the injection instant of 0.5 period of the stimulation signal.

32. (new) A method as claimed in Claim 25, wherein the operational simulation of each transistor of the logic cell comprises modeling the transistor connected to three voltage-controlled modeled voltage sources to allow an internal potential target of the transistor to be reached to be determined after injection, and connected to a modeled current source supplying an injection current proportional to a difference between the internal potential target and an internal potential at an injection instant.

33. (new) A method as claimed in Claim 32, wherein a first voltage source supplies at the injection instant the value of the internal potential of the transistor delayed by a period of the stimulation signal, and the second voltage source supplies the variation of the internal potential over a period, delayed by a half period of the stimulation signal, and a third voltage source supplies the internal potential target.

34. (new) A method as claimed in Claim 25, wherein an evolution of the internal potentials of the transistors of

the cell are determined from a static equilibrium state to a dynamic equilibrium state, relative to rising and falling transitions of the stimulation signal and for two initial values of the stimulation signal, and wherein the internal potentials of the transistors corresponding to the minimum and the maximum time delay of the cell are deduced therefrom.

35. (new) A method as claimed in Claim 25, further comprising:

determining an evolution of different time delays of the logic cell; and

determining minimum and maximum time delays.

36. (new) A method as claimed in Claim 25, further comprising:

determining an evolution of logic cell power consumption; and

determining minimum and maximum power consumption.

37. (new) A device for evaluating a CMOS logic cell manufactured in partially depleted silicon-on-insulation (PD-SOI) technology, the logic cell including transistors having a floating substrate, the device comprising:

modeling means for modeling the cell; and

processing means for determining internal potentials of the logic cell based on operational simulation of the modeled cell using a periodic stimulation signal, and for injecting the floating substrate of each transistor of the cell, at predetermined successive instants of injection, with

a charge proportional to a variation of the internal potential of the corresponding transistor determined during a predetermined time interval of the stimulation signal preceding the current injection instant to accelerate one of the charge and discharge of the floating substrate of the transistor.

38. (new) A device as claimed in Claim 37, wherein the processing means determines an injection current corresponding to the injected charge such that after injection the variation of the internal potential of the corresponding transistor reaches n times a measured variation of the internal potential.

39. (new) A device as claimed in Claim 38, wherein the processing means determines the value of n by measuring the variation of the internal potential of a transistor of the cell in a cycle of the stimulation signal and by an estimated amplitude of the variation of the internal potential of the transistor between a static equilibrium state and a dynamic equilibrium state.

40. (new) A device as claimed in Claim 37, wherein the processing means determines a proportionality coefficient by measuring the variation of the internal potential and from the charge variation of the transistor of the cell during a cycle of the stimulation signal, and of the injection duration.

41. (new) A device as claimed in Claim 37, wherein the stimulation signal comprises, in each period, a transition separating two plateaus, and wherein an injection instant takes place during a plateau at a transition distance, and the duration of injection of the current is selected to be greater than the time pitch of the operational simulation and less than the duration of a plateau.

42. (new) A device as claimed in Claim 37, wherein two consecutive injection instants are spaced by a period equal to two periods of the stimulation signal, and in the time interval has duration equal to a period of the stimulation signal.

43. (new) A device as claimed in Claim 42, wherein an initial instant of the time interval precedes the injection instant by 1.5 periods of the stimulation signal, at a final instant of the time interval precedes the instant of injection by 0.5 period of the stimulation signal.

44. (new) A device as claimed in Claim 37, wherein the modeling means comprises, for each transistor of the cell:

three modeled voltage-controlled voltage sources connected to the transistor, to allow an internal potential target of the transistor to be reached to be determined after injection; and

a modeled current source connected to the transistor to supply an injection current proportional to a difference between the internal potential target and the internal

potential at the instant of injection.

45. (new) A device as claimed in Claim 44, wherein a first voltage source supplies the injection instant, the value of the internal potential of the transistor delayed by a period of the stimulation signal, wherein a second voltage source supplies the variation of the internal potential over a period, delayed by a period of the stimulation signal, and wherein a third voltage source supplies the internal potential target.

46. (new) A device as claimed in Claim 37, wherein the processing means determines an evolution of the internal potentials of the transistors of the logic cell from a static equilibrium state to a dynamic equilibrium state, relative to rising and falling transitions of the stimulation signal and for two initial values of the stimulation signal, to deduce minimum and maximum internal potentials of the transistors.

47. (new) A device as claimed in Claim 46, wherein the processing means determines an evolution of different time delays of the cell, and determines minimum and maximum time delays.

48. (new) A device as claimed in Claim 47, wherein the processing means determines an evolution of power consumption of the logic cell, and determines minimum and maximum power consumption.

49. (new) A device for evaluating a CMOS logic cell manufactured in partially depleted silicon-on-insulation (PD-SOI) technology, the logic cell including transistors having a floating substrate, the device comprising:

a modeling unit to model the cell; and

a processor to determine internal potentials of the logic cell based on operational simulation of the modeled cell using a periodic stimulation signal, and to inject the floating substrate of each transistor of the cell, at predetermined successive instants of injection, with a charge proportional to a variation of the internal potential of the corresponding transistor determined during a predetermined time interval of the stimulation signal preceding the current injection instant to accelerate one of the charge and discharge of the floating substrate of the transistor.

50. (new) A device as claimed in Claim 49, wherein the processor determines an injection current corresponding to the injected charge such that after injection the variation of the internal potential of the corresponding transistor reaches n times a measured variation of the internal potential.

51. (new) A device as claimed in Claim 50, wherein the processor determines the value of n by measuring the variation of the internal potential of a transistor of the cell in a cycle of the stimulation signal and by an estimated amplitude of the variation of the internal potential of the transistor between a static equilibrium state and a dynamic equilibrium state.

52. (new) A device as claimed in Claim 49, wherein the processor determines a proportionality coefficient by measuring the variation of the internal potential and from the charge variation of the transistor of the cell during a cycle of the stimulation signal, and of the injection duration.

53. (new) A device as claimed in Claim 49, wherein the modeling unit comprises, for each transistor of the cell:

three modeled voltage-controlled voltage sources connected to the transistor, to allow an internal potential target of the transistor to be reached to be determined after injection; and

a modeled current source connected to the transistor to supply an injection current proportional to a difference between the internal potential target and the internal potential at the instant of injection.